REMARKS

Claims 1-7, all the claims pending in the application, stand rejected. Applicants have amended claim 1 in order to overcome a rejection under Section 112, second paragraph, and the prior art rejection.

Claim Rejection - 35 U.S.C. § 112

Claims 1-7 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is traversed for at least the following reasons.

The Examiner notes that claim 1 recites the limitation "the current source" but refers to first and second current sources. Thus, the Examiner cannot determine which source is intended.

Applicant has amended the claim in order to remedy this error by referring to the "first and second constant current sources." The rejection of claims 2-7 would also be overcome by this amendment.

Claim Rejections - 35 U.S.C. § 103

Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cabler (5,625,357) in view of Ledzius et al (5,323,157). Applicants respectfully traverse this rejection for at least the following reasons.

At pages 3-5 of the Office Action, the Examiner has changed the previous basis for rejection of claims 1-7 as being unpatentable over Cabler (5,625,357) in view of Ledzius et al (5,323,157). Previously, the Examiner relied upon the circuitry of Fig. 2 for the rejection, but now looks to Fig. 1. At page 2 of the Office Action, in the Response to Arguments section, the Examiner addresses the several arguments for patentability raised in the previous Amendment.

First the Examiner notes Applicant's arguments that Cabler fails to teach two constant current sources. The Examiner now points to Fig. 1 of Cabler and asserts that the FIR (50) comprises two sources I_0 and I_1. The Examiner is correct with regard to Fig. 1 of Cabler. Notably, there is only one current source I_{REF} illustrated in the remaining Figures of Cabler, and the use of only one current source is a key feature of the embodiments illustrated in Figs. 2, 3 and 5A-5C. As previously asserted by the Applicant, these figures illustrate two current paths that are directed through two resistances R_0 and R_1 and carry different currents, I_0 and I_1, but

there is only one current source. Thus, only the teachings of Fig. 1 in Cabler with respect to the remaining limitations in the claim need be considered.

In Fig. 1 of Cabler, the Sigma-delta 16 provides plural control bits B_0-B_N on line 12 to shift register 14. The shift register 14 provides "N" outputs B_0, B_1, B_2 etc., as explained at col. 1, lines 38-54. As is seen in Fig. 1, there is one current source for **each** shift register output, as is clear from the outputs B_0, B_1, B_2 etc. and the corresponding current sources I_0, I_1, etc. Similarly, there is a corresponding non-inverted switch B_0, B_1 etc. and inverted switch B0, B_1, etc for each current switch. Thus, the circuit in Cabler requires more than two current sources and more than two dedicated pairs of inverted and non-inverted switches, one for each bit B_0-B_N. All of the outputs from the non-inverted switches B0-B_N flow to non-inverted output 62 and all of the outputs from the inverted switches B0-B_N will flow to inverted output 58.

By contrast, in the present invention, there are only two constant current sources, one for the non-inverted line and one for the inverted line into the differential amplifier of current to voltage circuit 6. Each current source is coupled to a plurality of MOS transistor circuits (T1-Tn), each MOS transistor circuit having a pair of inverted an non-inverted outputs. This arrangement has the advantage of reduced components and simplified circuitry.

In order to clarify that there are only two constant current sources and that more than two switches control such currents, claim 1 has been amended to state that there are "n" elements (where n is a whole number greater than 2). Clearly, this limitation is taught in Fig. 1 of the present application, where switches T_1, T_2 - T_n are illustrated. This feature clearly distinguishes over the structure of Cabler.

Ledzius does not remedy this deficiency in Cabler. Ledzius is cited merely for its teaching in Fig. 3 of a sigma delta DAC including a plurality of flip-flops (81-83) used as delay elements, each flip flop having two outputs, each coupled to a respective one MOS transistor, as illustrated in Fig. 4. Ledzius teaches plural current sources for respective flip flops, as illustrated in Fig. 3. This would not teach or suggest the structure, as now claimed.

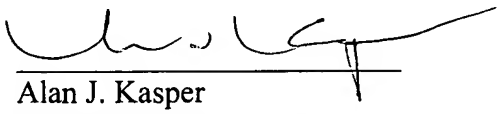
In sum, there is no other teaching or suggestion in any of the cited prior art references that would lead to the structure as now recited in claim 1. Thus, claim 1, as now directed to an output filter for a delta sigma modulator that comprises (1) first and second constant current

source [8a, 8b] and (2) an FIR filter [4], where the FIR filter recited in the claim has (a) a plurality of delay elements [F_1-Fn] arranged in cascade, where n is a whole number greater than two, and where (b) each element is operative to output data from the delta sigma modulator [2] by controlling currents via n switches from the constant current source on the basis of each of the output data. As a result, a plurality of weighted currents, that are weighted according to a filter characteristic, are generated. The weighted currents are added and outputted in an output side of the FIR filter.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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